Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application.

Listing of the Claims:

Claims 1-2 (canceled)

Claim 3 (previously presented): The system of claim 22

wherein each photocell generates a light signal and a reset signal;

wherein the sequential readout circuit determines a difference between the light signal and the reset signal for each photocell in the array in a time sequential manner.

Claim 4 (canceled)

Claim 5 (previously presented): The system of claim 22 further comprising:

an integration capacitor having a first electrode for coupling to the input of the amplifier and a second electrode for coupling to the output of the amplifier;

wherein the amplifier includes a charge transfer mode and a unity gain mode.

Claim 6 (previously presented): The system of claim 22 wherein the sequential readout circuit includes

a level shifting circuit that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing level shifting of the output of the amplifier.

Claim 7 (previously presented): The system of claim 22 wherein the sequential readout circuit includes

a gain manipulation circuit that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing gain manipulation of the amplifier.

Claim 8 (previously presented): The system of claim 22 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claims 9-10 (canceled)

Claim 11 (previously presented): The sequential readout circuit of claim 23

wherein the amplifier determines the difference between the light signal and the reset signal for the photocells in the array in a time sequential manner.

Claims 12-13 (canceled)

Claim 14 (previously presented): The sequential readout circuit of claim 23

wherein the amplifier includes a charge transfer mode, a unity gain mode, a first input; and an output; and

wherein the circuit further includes an integration capacitor having a first electrode for coupling to the negative input terminal and a second electrode for coupling to the output terminal of the amplifier.

Claim 15 (previously presented): The sequential readout circuit of claim 23 further comprising:

a level-shifting mechanism that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing level shifting of the output of the amplifier.

Claim 16 (previously presented): The sequential readout circuit of claim 23 further comprising:

a gain mechanism that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing gain manipulation of the amplifier.

Claim 17 (previously presented): The sequential readout circuit of claim 23 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claims 18-21 (canceled)

Claim 22 (previously presented): A system comprising:

a) an array of photocells that are arranged in rows and columns; and

b) a sequential readout circuit for sequentially reading out the value of the photocells one photocell at a time; wherein the sequential readout circuit includes;

a first sampling circuit that includes a first electrode for coupling to a first column and a second electrode;

a first switch that includes a first electrode coupled to the second electrode of the first sampling circuit, a second electrode, and a third electrode for receiving a first sample control signal; wherein the first switch selectively couples the first electrode of the first switch to the second electrode of the first switch when the first sample control signal is asserted; wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column;

a second sampling circuit that includes a first electrode for coupling to a second column and a second electrode;

a second switch that includes a first electrode coupled to the second electrode of the second sampling circuit, a second electrode, and a third electrode for receiving a second sample control signal; wherein the second

switch selectively couples the first electrode of the second switch to the second electrode of the second switch when the second sample control signal is asserted; wherein the second sampling circuit samples a light signal and a reset signal from each photocell in the second column; and

an amplifier that includes a negative input terminal coupled to the second electrode of the first switch and the second electrode of the second switch; wherein the amplifier includes an output terminal for generating a signal that corresponds to the amount of light received by a particular photocell in the array.

Claim 23 (previously presented): A sequential readout circuit for coupling to an array of photocells that includes a plurality of photocells that are arranged in rows and columns, each photocell generating a light signal during a first period of time that represents received light and a reset signal after being reset, the sequential readout circuit comprising:

a first sampling circuit that includes a first electrode for coupling to a first column and a second electrode;

a first switch that includes a first electrode coupled to the second electrode of the first sampling circuit, a second electrode, and a third electrode for receiving a first sample control signal; wherein the first switch selectively couples the first electrode of the first switch to the second electrode of the first switch when the first sample control signal is asserted; wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column;

a second sampling circuit that includes a first electrode for coupling to a second column and a second electrode;

a second switch that includes a first electrode coupled to the second electrode of the second sampling circuit, a second electrode, and a third electrode for receiving a second sample control signal; wherein the second switch selectively couples the first electrode of the second switch to the second electrode of the second switch when the second sample control signal is asserted; wherein the second sampling circuit samples a light signal and a reset signal from each photocell in the second column;

an amplifier that includes a negative input terminal coupled to the second electrode of the first switch and second electrode of the second switch; wherein the amplifier includes an output terminal for generating a signal that corresponds to the amount of light received by a particular photocell in the array.

Claim 24 (previously presented): The sequential readout circuit of claim 23 wherein the sequential readout circuit sequentially reads out a value of the photocells one photocell at a time

Claim 25 (previously presented): The system of claim 22 wherein the sequential readout circuit measures a light signal from a photocell, measures a reset signal from a photocell, and stores a charge that represents the difference between the light signal and the reset signal.

Claim 26 (previously presented): The sequential readout circuit of claim 23 wherein the sequential readout circuit measures the light signal from a photocell, measures the reset signal from a photocell, and stores a charge that represents the difference between the light signal and the reset signal.

Claim 27 (previously presented): The system of claim 22 wherein the first sampling circuit includes a sampling capacitor.

Claim 28 (previously presented): The system of claim 22 wherein the second sampling circuit includes a sampling capacitor.

Claim 29 (previously presented): The sequential readout circuit of claim 23 wherein the first sampling circuit includes a sampling capacitor.

Claim 30 (previously presented): The sequential readout circuit of claim 23 wherein the second sampling circuit includes a sampling capacitor.

Claim 31 (previously presented): A method for reading out values of an array of photocells that are arranged in rows and columns comprising:

sampling the light signal of all the photocells in a first row by utilizing a sampling circuit that corresponds to a particular column of the array;

holding the light signal;

after the photocells of the first row have been reset, sampling the reset signals of photocells of the first row by using the sampling circuit;

determining a difference between the light signal and the reset signal of a first photocell in the first row by utilizing a charge conversion circuit that is coupled to the sampling circuit; and

sequentially reading out the values of the array of photocells.